Finite Element Modeling of Heat Transfer and Thermal Stresses for Three-dimensional Packaging of Power Electronics Modules

Simon S. Wen and Guo-Quan Lu
Center for Power Electronics Systems
The Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University, Blacksburg, VA 24061-0111
Phone: 1-540-231-9467 Fax: 1-540-231-9467
E-mail: swen@vt.edu

Abstract-The state-of-the-art packaging technology for power electronics modules uses wire bonds to interconnect power devices. Emerging 3-D interconnected power package designs have shown their advantages over conventional wire bonding modules in higher power density, reduced interconnect resistance and parasitic oscillations, better thermal management, higher level of system integration and lower cost. Our attempt to eliminate the use of wire bonds has led to the development of a three-dimensional, stacked-plate technique. With this technique, thick metal posts are directly soldered onto power devices to form an interconnected 'flat-pack' package that potentially offers improved electrical and thermal performance. On the other hand, high-density 3-D power modules experience more stringent environmental conditions such as thermal cycles during the fabrication and operation. Due to different thermal expansion coefficients (CTE) in different materials, cyclic stresses may lead to thermal fatigue and failure of power modules. A study in this respect will help understanding the key issues of thermal management and thermo-mechanical reliability for 3-D power electronic packaging. In this paper, we present a finite-element modeling of thermal and thermomechanical behavior in a power module fabricated by this technique.

Key words: modeling, power electronics packaging

1. Introduction

Various emerging novel power packaging technologies have shown the very promising future in electrical, thermal, and mechanical aspects. Some of these technologies replace conventional wire bonding with copper interconnect. This approach requires the availability of solderable power devices, or involves the processing of surface metallization, such as International Rectifier's CopperStrap technology[1] and General Electric's Power Overlay Technology (POL)[2]. In our work, we have explored the assembly of high power modules using a stacked plate structure interconnected by copper posts. Integration of high power density, compact 3D power modules is rather challenging due to the complicated nature of the fabrication process. The thermal cycle loading and thus thermal stresses occurring throughout the whole lifetime of power modules, which constitute a large part of the module failure modes[3]. Therefore, the thermal and thermo-mechanical design and evaluation are crucial.

The complexity of thermo-mechanical behavior of power electronic modules requires that a nonlinear finite element analysis procedure be used. Using a 3D FEM, we performed an analytical determination of the temperature distribution over the power modules during power loading stage, and calculated the thermal resistance and the thermal stress using the obtained temperature field.

2. Module Description

The module is a half-bridge with two high power IGBT switches (rated 1200V, 75A) and two high power diodes (rated at 1200V, 75A) sandwiched between two DBC (Direct bonded copper) substrates. Total power loss of this module was estimated to be 800 Watts. Instead of using wire bonding, copper posts were used to interconnect the devices to the circuit. Double-sided cooling scheme thus could be enabled when necessary, especially in high power application. The geometry of the assembly is shown in Fig. 1, lower.

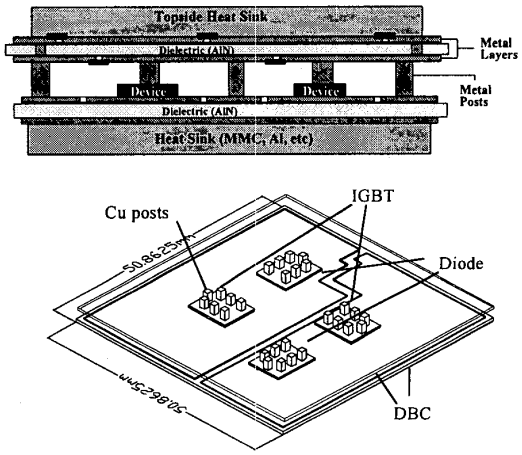

Fig. 1. Interconnect scheme (upper) and the geometry of the 3-D power module (lower).

3. Finite Element Analysis Procedure

3.1 Material Properties

Nonmetallic materials in this model, such as aluminum nitride and semiconductor silicon device were assumed to be linear elastic. Copper was assumed to be elastic-plastic since the residual stress within the DBC substrate may exceed its yielding point. To simplify the modeling without losing the insight to the problem, copper's plasticity property was modeled as perfect plastic, i.e. as soon as the stress exceeds the yield strength of copper, the stress will keep at that level with no hardening effects. The 63Sn37Pb eutectic solder was assumed to be viscoplastic since it is widely believed that rate dependent plasticity (creep) occurs in the solder over time. The Garofalo hyperbolic sine law (1) was applied to model the creep behavior of the solder joints, which has been found to cover the intermediate and high stress regimes,

$$\dot{\varepsilon}^{cr} = A(\sinh B\sigma)^n \exp(-\frac{\Delta H}{RT}) \qquad (1)$$

Where ε^{cr} is the equivalent uniaxial tensile creep strain, σ is the equivalent uniaxial tensile stress, T is the absolute temperature in K, and A, B, n (stress exponent), and ΔH (activation energy) are input constants[4], and R is the gas constant. The elastic modulus, Poisson Ratio, yield strength and CTE of the solder were modeled as temperature dependent using the data given by Hong. Relevant material properties and constants of the package components are shown in Table 1. And the creep properties of the 63Sn37Pb solder are listed in Table 2.

Table 1. Mechanical properties of packaging materials

Materials		Cu	AlN	Si	63Sn37Pb		
Density	Kg/m^3	8930	3260	2330	8470		
Modulus	GPa	135	330	130	26.4	12.5	6.9
Poisson ratio		0.34	0.23	0.28	.36	.365	.378
Yield strength	MPa	138			36.4	15.2	9.6
CTE	ppm /K	17	4.5	4.1	25.2	26.1	27.3
Reference Temperature	K	273	273	273	273	323	373

Table 2. Visco-plastic properties of eutectic solder

Creep Constants for Hyperbolic Law				
A (1/sec)	B (1/Pa)	n	ΔH (J/mol)	**R** (J/mol·K)
12423	0.126E-6	1.89	61417	8.314

3.2 Finite Element Analysis Steps

In this model, the component dimensions are drastically different among different components. To finely mesh the whole model using the smallest characteristic element length is very expensive in terms of time and computer resource. It will be more effective to finely mesh only the power IGBT devices and the posts, where the stress concentration is most likely to occur, and coarsely mesh the other part of the substrate and components. The final mesh includes 6538 HEX elements, 8 grounded spring elements and 9368 nodes.

In thermal analysis, the model was applied an equivalent convective heat transfer coefficient of 20,000 W/m^2°C (equivalent to a heat sink thermal resistance of 0.05 °C/W. Each IGBT chip dissipates 300 watt and the diode dissipates 100 watt. In the structural analysis, the model was constrained in the normal direction on the bottom nodes of the DBC substrate. Eight grounded spring elements were loaded to the four corner nodes on the bottom DBC substrate, constraining the x and y direction, to prevent the model from rigid body motion. The stiffness of these spring elements was very small so that their addition would not affect the structural analysis results.

The modeling was intended to describe the thermo-mechanical response after the devices were powered up with the consideration of the residual stress from the soldering process. Therefore three steps of modeling were needed:

- Steady state heat transfer analysis to obtain the temperature profile resulting from the power dissipation of the power chips
- Nonlinear static analysis and creep analysis to calculate the residual stress in the module after the soldering processing
- Nonlinear static analysis and creep analysis to evaluate the thermo-mechanical response, considering the residual stress from step 2, and using the temperature results from step 1 as the thermal load

4. Finite Element Modeling Results

4.1 Thermal Results for Power Loading Stage

The temperature distribution of the module is shown in Fig. 2.

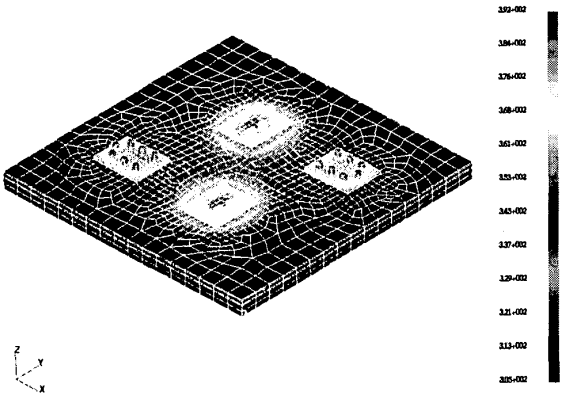

Fig. 2. Temperature distribution in the 3-D power module.

The maximum junction temperature in the module is 119° C (392 K). The maximum temperature occurs in IGBT chips. The diode chips have a maximum temperature of 72°C (345 K). The thermal resistance between the junction and the case (here 'case' refers to the coldest region in top DBC substrate) is defined as:

$$R = \frac{T_j - T_c}{Q} \qquad (2)$$

where T_j is the maximum junction temperature, T_c is the case temperature, and Q is the chip power loss. For IGBT chip, T_j is 119°C and T_c is 32°C, and the power loss is 300 watt. Thus in this model the thermal resistance of IGBT chip is about 0.29°C/W. Thermal resistance of the diode chip is calculated to be 0.4 °C/W. In commercial high power IGBT module, IGBT chip junction-to-case thermal resistance is about 0.3°C/W and this value is about 0.6°C/W for diode chip[5]. From modeling results, the 3-D power module shows a better thermal performance.

With heat sink attached only on the bottom of heat spreader, since the heat dissipation of IGBT chip is three times that of the diode chip, heat also takes the path from IGBT chips to top DBC through copper posts, and flows back down to diode chips through the copper posts. In other words, cooling of the stacked-plate structure power module is more efficient since the heat flow reduces the heat crowding at the IGBT region by redirecting the excessive heat to diode chips.

In order to more clearly demonstrate this point, Fig. 3 show the local heat flux vector plot in the module. The copper posts help distribute heat flow more uniform through the top heat flow path. The upward stream of heat flux in IGBT posts and downward stream in diode posts can be seen clearly.

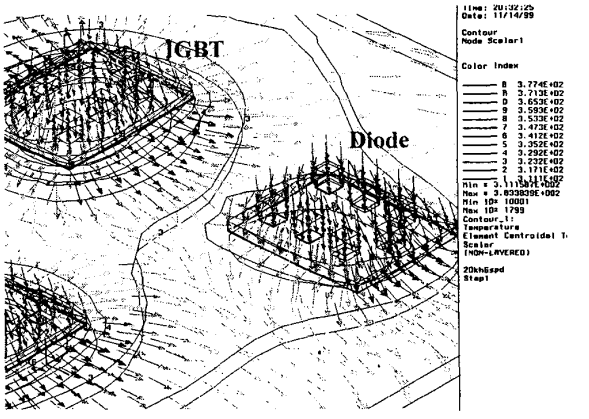

Fig. 3. Heat flux vector plot in the 3-D power module.

The maximum heat flux in the module is 540 W/m^2, which is crowded around the IGBT device-to-DBC region.

The posts have clearly showed its function of an added thermal path. On the top DBC substrate, however, we can add another heatsink. Further improvement in the thermal management is therefore expected. With an added heat sink (also has a thermal resistance of 0.05°C/W) on the top DBC substrate, a significant reduction of junction temperature has been observed. Maximum chip temperature has reduced 11°C than that of single-side cooled module.

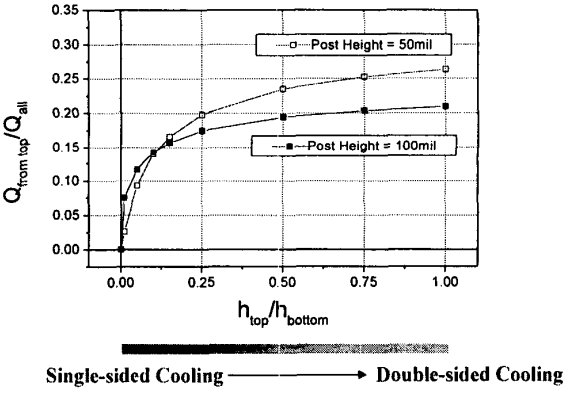

Fig. 4. Double-sided cooling effects and post height effects.

A series of modeling have been performed to evaluate the effect of additional heat sink on top. Fig. 4 shows how an added heat sink on top can share the heat flow in percentage. The modeled thermal resistance for the bottom heat sinks has been kept at 0.05 °C /W, and the top heat sink thermal resistance changes from 5°C/W to 0.05°C/W (from left to right). The per cent of heat dissipated by top heat sink shows an increase when its thermal resistance approaches that of the bottom heat sink. Copper post height effects are also evaluated as shown in the same figure (Fig. 4). With the

copper post-heat removal path occupying only 10% of the overall heat generation area, 30% of total heat dissipation flows to the top plate.

4.2 Thermal Stress and Creep Analysis

Figure 3 highlights the residual stress distribution after the module was cooled down from soldering temperature 183°C to room temperature 27°C. As expected, maximum stress occurred within the AlN DBC substrate. This results from the fact that the CTE difference between AlN and copper is 12.5×10^{-6}/°C. Although copper post and silicon device have a similar CTE mismatch, the solder served as a buffer layer and released the stress concentration between the posts and the device.

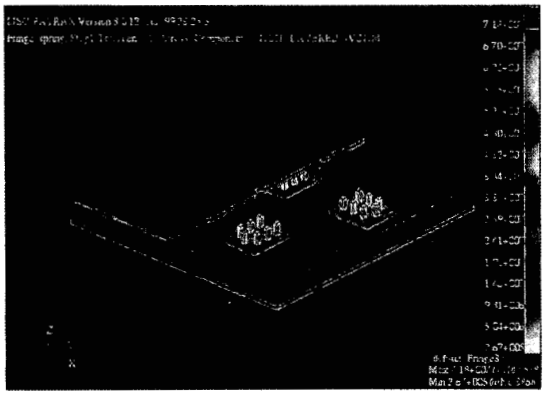

Fig. 5. Residual stress after soldering process.

The residual stress on the devices was actually reduced due to the creep behavior of the solder alloy. Figure 4 shows that after 2 seconds' creep analysis, the residual stress on the devices has been lowered by a factor of 2.

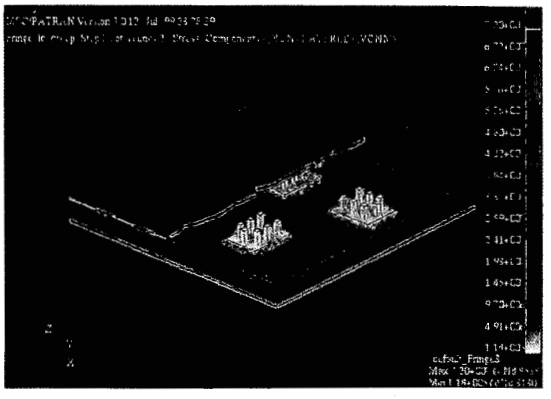

Fig. 6. Residual stress after creep analysis.

The direct effect of power loading is the large spatial variation of temperature within power modules. Unlike the isothermal change in soldering process, the temperature could be very localized in some area and this may lead to even worse stress concentration.

Figure 6 shows the Von Mises stress distribution of the module after being powered up. With the highest stress still in the DBC substrates, the temperature made the difference between IGBTs and Diodes. Higher temperature gradient across the IGBT resulted in more thermal stresses.

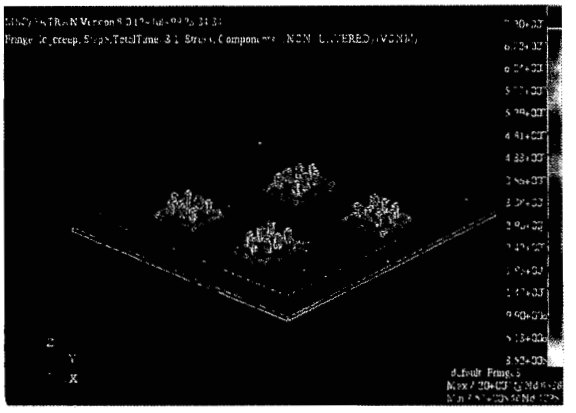

Fig. 7. Von Mises stress distribution in the module after being powered up.

Again, if considering the creep behavior of the solder alloy, the concentrated stresses in the devices would be partially released, as shown in Figure 7. Excessive stress was reduced from rigid components that are sandwiched between the solder on both substrates, such as the silicon chips and copper post.

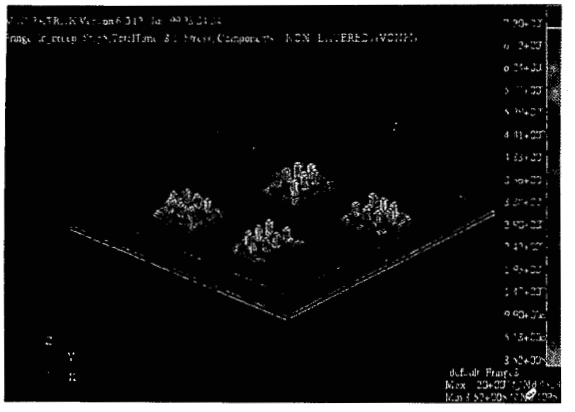

Fig. 8. Creep released the stress concentration at the post-device interface.

Meanwhile, the stress in the DBC substrate underneath the power chips has reached 56MPa. This value has exceeded the yield strength of 63Sn37Pb solder at this temperature thus large amount of plastic strain is present in that solder layer.

The strain fringe from nonlinear static analysis in the devices, solders, posts and DBC were also plotted and shown in Figure 9. The highest strain occurred mostly in the solder interface between the power chips and DBC. This amount of strain includes elastic strain due to the linear response of the materials, thermal strain due to CTE mismatch of materials, and inelastic strain due to the thermal stress exceeded the yielding point of solder.

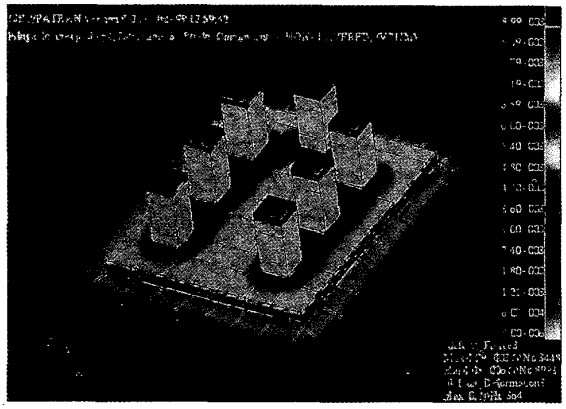

Fig. 9. Strain distribution in the module after being powered up.

In Figure 10, the strain distribution is plot with the same scale as Figure 9 indicating that by including the effect of the rate dependent plasticity of solder reduced the strains in devices.

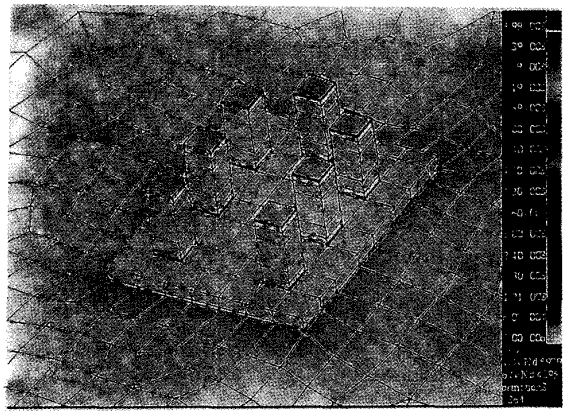

Fig. 10. The strain distribution in the module if considering creep effects.

The Von Mises stress in different locations among the IGBT and diode was listed in Table 3. Apparently the stress in solder joint between copper posts and power chips were close to each other for IGBT and diode. In both cases the stress was below the yield strength of solder at the working temperature. The stress in the center of the chip was several times larger than that in the corner. After the module was powered up, stress increase in the IGBT was larger than that in the diode because the temperature variation in IGBT is larger than that of the diode.

Table 3. Von Mises stress in IGBTs and Diodes.

Unit: MPa		Chip Center	Chip Corner	Solder in between posts and chips
Residual Stress	IGBT	8.27	3.43	5.06
	Diode	6.65	1.8	6.0
Stress in power stage	IGBT	15.4	5.05	8.2
	Diode	11.5	3.4	8.3

Under the thermal stress, the copper posts and other components had a specific amount of deformation and displacement relative to their original shape and position. Fig. 11 shows an exaggerated picture of the deformed shape of the IGBT posts at the power stage. The module center is to the bottom of this picture. The displacement of the posts indicates that during locally power heating, the post underwent a displacement toward the edge of the module. This is because that the top plate was hotter than the bottom plate due to lack of a heat sink thus had a larger expansion, which forced the posts to deform in that way.

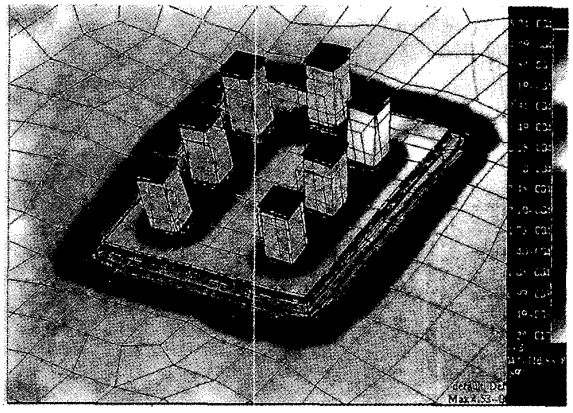

Fig. 11. Exaggerated deformation plot of IGBT during power stage.

4.3 Discussion And Future Work

Some assumptions were implicitly made with this analysis. Materials were perfectly uniform and isotropic, and interface bonding was also perfect. Various defects within materials and interfaces in the real case, which could have sometimes very large impact on the module, were ignored. The structural analysis requires a more detailed study in the critical region to give a quantitatively characterization. Future work would be focused on using CFD to determine local heat transfer, and the modeling of thermal and power cycling, thermal fatigue and life prediction with experimental verification.

5. Conclusion

In this study thermal and thermally induced response of a 3-D power modules packaged by a stacked plate structure was investigated using Finite Element Method. It has been found that the copper post interconnects serve as an added heat removal path and improve the thermal performance of the module. The thermo-mechanical stresses were also qualitatively studied. The solder materials help the chips release part of the stress concentration due to their creep behavior.

Acknowledgement

This work was supported by the Office of Naval Research. This work also made use of ERC Shared Facilities supported by the National Science Foundation under Award Number EEC-9731677.

References

[1] International Rectifier, their website at http://www.irf.com/_FKK4aEd/whats-new/powireview99fa.pdf

[2] Burhan Ozmat, et al., "A New Power Module Packaging Technology for Enhanced Thermal Performance", International Conference on Thermal, Mechanics and Thermomechanical Phenomena in Electronic Systems, Las Vegas, Nevada, USA, May 23-26, 2000.

[3] J. H. Lau, "Solder Joint Reliability of Flip Chip and Plastic Ball Grid Array Assemblies Under Thermal, Mechanical, and Vibrational Conditions," IEEE Trans. CPMT- Part B, Vol. 19, NO. 4, pp. 728-735, Nov. 1996.

[4] B. Z. Hong, "Thermal Fatigue Analysis of a CBGA Package with Lead-free Solder Fillets," Proceedings of 1998 InterSociety Conference on Thermal Phenomena, Seattle, Washington, May 27-30, 1998.

[5] IXYS Corp., their website at http://www.ixys.com

[6] C. V. Godbold, V. A. Sankaran, and J. L. Hudgins, "Novel Design in Power Modules," Proceedings of the 30th Industry Applications Society, Vol. I, pp. 911-915, Oct 8-12, 1995.